IN THE CLAIMS

Please amend the claims as follows. Any other difference between the claims below and the prior state of the claims is unintentional and in the nature of a typographical error.

1. (Currently Amended) A semiconductor apparatus comprising ~~at least one~~ a double poly bipolar transistor and ~~at least one~~ a double poly metal oxide semiconductor (MOS) transistor; [[,]]

wherein a first polysilicon layer comprises a base of the double poly bipolar transistor and a gate of the double poly MOS transistor;

wherein a second polysilicon layer separate from the first polysilicon layer comprises an emitter of the double poly bipolar transistor and a source/drain of the double poly MOS transistor;

wherein [[a]] the base of the double poly bipolar transistor ~~contains~~ comprises a first dopant having a first dopant concentration, and wherein the [[a]] gate of the double poly ~~metal oxide semiconductor~~ MOS transistor ~~contains~~ comprises the ~~said~~ first dopant having the ~~said~~ first dopant concentration; and

wherein [[an]] the emitter of the double poly bipolar transistor ~~contains~~ comprises a second dopant having a second dopant concentration, and wherein [[a]] the source/drain of the double poly ~~metal oxide semiconductor~~ MOS transistor ~~contains~~ comprises the ~~said~~ second dopant having the ~~said~~ second dopant concentration.

~~; wherein said semiconductor apparatus further comprises a first polysilicon layer and a~~

~~second silicon layer that is separate from the first polysilicon layer.~~

2. (Currently Amended) The semiconductor apparatus as set forth in Claim 1, wherein:

~~said at least one double poly bipolar transistor and said at least one double poly metal oxide semiconductor (MOS) transistor comprise a substrate and a first layer of polysilicon (Poly1) material wherein:~~

the first polysilicon layer comprises first polysilicon layer material in the double poly bipolar transistor and first polysilicon layer material in the double poly MOS transistor;

~~said~~ the first ~~layer of~~ polysilicon layer ~~(Poly1)~~ material in ~~said at least one~~ the double poly bipolar transistor ~~is doped with~~ comprises impurity ions of ~~said~~ the first dopant [[to]] forming the base of the double poly bipolar transistor, the base comprising an extrinsic base; and

~~said~~ the first ~~layer of~~ polysilicon layer ~~(Poly1)~~ material in ~~said at least one~~ the double poly MOS transistor ~~is doped with~~ comprises impurity ions of ~~said~~ the first dopant [[to]] forming the gate of the double poly MOS transistor ~~a MOS transistor gate~~.

3. (Currently Amended) The semiconductor apparatus as set forth in Claim 2, wherein:

~~said at least one~~ the double poly bipolar transistor is a PNP transistor; and ~~wherein~~ ~~said at least one~~ the double poly MOS transistor is an NMOS transistor.

4. (Currently Amended) The semiconductor apparatus as set forth in Claim 2, wherein:

~~said at least one~~ the double poly bipolar transistor is an NPN transistor; and ~~wherein~~ ~~said at least one~~ the double poly MOS transistor is a PMOS transistor.

5.-6. (Cancelled)

7. (Currently Amended) The semiconductor apparatus as set forth in Claim 2, ~~wherein~~ further comprising:

a substrate;

~~said substrate is implanted with~~ impurity ions of a third dopant in the substrate [[to]] forming an intrinsic base ~~in said at least one~~ of the double poly bipolar transistor; and

~~said substrate is simultaneously implanted with~~ impurity ions of ~~said~~ the third dopant in the substrate [[to]] forming a lightly doped drain ~~in said at least one~~ of the double poly MOS transistor.

8. (Currently Amended) The semiconductor apparatus as set forth in Claim 7, wherein ~~said~~ the lightly doped drain ~~in said at least one~~ of the double poly MOS transistor is self aligned.

9. (Currently Amended) The semiconductor apparatus as set forth in Claim 7, wherein:

~~said at least one~~ the double poly bipolar transistor is a PNP transistor; and ~~wherein~~ ~~said at least one~~ the double poly MOS transistor is an NMOS transistor.

10. (Currently Amended) The semiconductor apparatus as set forth in Claim 7, wherein:

~~said at least one~~ the double poly bipolar transistor is an NPN transistor; and ~~wherein~~ ~~said at least one~~ the double poly MOS transistor is a PMOS transistor.

11.-12. (Cancelled)

13. (Currently Amended) The semiconductor apparatus as set forth in Claim 7, wherein:

~~said at least one double poly bipolar transistor and said at least one double poly metal oxide semiconductor (MOS) transistor further comprise a second layer of polysilicon (Poly2) material wherein:~~

the second polysilicon layer comprises second polysilicon layer material in the double poly bipolar transistor and second polysilicon layer material in the double poly MOS transistor;

~~said~~ the second ~~layer of~~ polysilicon layer ~~(Poly2)~~ material in ~~said at least one~~ the double poly bipolar transistor ~~is doped with~~ comprises impurity ions of ~~said~~ the second dopant [[to]] forming the [[an]] emitter of the double poly bipolar transistor; and

~~said~~ the second ~~layer of~~ polysilicon layer ~~(Poly2)~~ material in ~~said at least one~~ the double poly MOS transistor ~~is simultaneously doped with~~ comprises impurity ions of ~~said~~ the second dopant [[to]] forming the ~~a MOS~~ source/drain of the double poly MOS transistor.

14. (Currently Amended) The semiconductor apparatus as set forth in Claim 13, wherein ~~said~~ the emitter ~~in said at least one~~ of the double poly bipolar transistor is self aligned to [[an]] the extrinsic base of ~~said at least one~~ the double poly bipolar transistor.

15. (Currently Amended) The semiconductor apparatus as set forth in Claim 13, wherein ~~said MOS~~ the source/drain ~~in said at least one~~ of the double poly MOS transistor is self aligned to [[a]] the gate of ~~said at least one~~ the double poly MOS transistor.

16. (Currently Amended) The semiconductor apparatus as set forth in Claim 13, wherein ~~said~~ the second ~~layer of~~ polysilicon layer ~~(Poly2)~~ material in ~~said at least one~~ the double poly bipolar transistor ~~is simultaneously doped with~~ further comprises impurity ions of ~~said~~ the second dopant [[to]] forming a deep collector of the double poly bipolar transistor.

17. (Currently Amended) The semiconductor apparatus as set forth in Claim 13, wherein ~~said MOS~~ the source/drain in ~~said~~ the second ~~layer of~~ polysilicon layer ~~(Poly2)~~ material in ~~said at least one~~ the double poly MOS transistor ~~is etched to~~ comprises separate ~~said MOS source/drain into a~~ source and [[a]] drain regions.

18.-19. (Cancelled)

20. (Currently Amended) The semiconductor apparatus as set forth in Claim 13, wherein:

~~said at least one~~ the double poly bipolar transistor is an NPN transistor; and ~~wherein~~ ~~said at least one~~ the double poly MOS transistor is a PMOS transistor.

21. (Currently Amended) The semiconductor apparatus as set forth in Claim 13, wherein:

~~said at least one~~ the double poly bipolar transistor is a PNP transistor; and ~~wherein~~ ~~said at least one~~ the double poly MOS transistor is an NMOS transistor.

22.-42. (Cancelled)

43. (Currently Amended) A semiconductor apparatus comprising ~~at least one~~ a double poly bipolar transistor and ~~at least one~~ a double poly metal oxide semiconductor (MOS) transistor;

wherein a base of the double poly bipolar transistor ~~contains~~ comprises a first dopant having a first dopant concentration, and wherein a gate of the double poly MOS transistor ~~contains said~~ comprises the first dopant having ~~said~~ the first dopant concentration; and

wherein an emitter of the double poly bipolar transistor ~~contains~~ comprises a second dopant having a second dopant concentration, and wherein a source/drain of the double poly MOS transistor ~~contains said~~ comprises the second dopant having ~~said~~ the second dopant concentration.

44. (Currently Amended) The semiconductor apparatus as set forth in Claim 43, wherein:

~~said at least one~~ the double poly bipolar transistor and ~~said at least one~~ the double poly MOS transistor comprise ~~a substrate and~~ a first layer of polysilicon material; ~~, wherein:~~

~~said~~ the first layer of polysilicon material in ~~said at least one~~ the double poly bipolar transistor ~~is doped with~~ comprises impurity ions of ~~said~~ the first dopant [[to]] forming the base of the double poly bipolar transistor, the base comprising an extrinsic base; and

~~said~~ the first layer of polysilicon material in ~~said at least one~~ the double poly MOS transistor ~~is doped with~~ comprises impurity ions of ~~said~~ the first dopant [[to]] forming the gate of the double poly MOS transistor ~~a MOS transistor gate~~.

45. (Currently Amended) The semiconductor apparatus as set forth in Claim 44, wherein:

~~said at least one~~ the double poly bipolar transistor and ~~said at least one~~ the double poly MOS transistor further comprise a second layer of polysilicon material; ~~, wherein:~~

~~said~~ the second layer of polysilicon material in ~~said at least one~~ the double poly bipolar transistor ~~is doped with~~ comprises impurity ions of ~~said~~ the second dopant [[to]] forming [[an]] the emitter of the double poly bipolar transistor; and

~~said~~ the second layer of polysilicon material in ~~said at least one~~ the double poly MOS transistor ~~is simultaneously doped with~~ comprises impurity ions of ~~said~~ the second dopant [[to]] forming the ~~a MOS~~ source/drain of the double poly MOS transistor.

46. (Currently Amended) The semiconductor apparatus as set forth in Claim 45, ~~wherein~~ further comprising:

a substrate;

~~said substrate is implanted with~~ impurity ions of a third dopant in the substrate [[to]] forming an intrinsic base ~~in said at least one~~ of the double poly bipolar transistor; and

~~said substrate is simultaneously implanted with~~ impurity ions of ~~said~~ the third dopant in the substrate [[to]] forming a lightly doped drain ~~in said at least one~~ of the double poly MOS transistor.

47. (Currently Amended) The semiconductor apparatus as set forth in Claim 45, wherein ~~said~~ the second layer of polysilicon material in ~~said at least one~~ the double poly bipolar transistor ~~is simultaneously doped with~~ further comprises impurity ions of ~~said~~ the second dopant [[to]] forming a deep collector of the double poly bipolar transistor.

48. (New) An apparatus comprising:

a semiconductor substrate;

a first polysilicon layer over the substrate; and

a second polysilicon layer over the first polysilicon layer;

wherein the first polysilicon layer comprises an extrinsic base of a double poly bipolar transistor and a gate of a double poly metal oxide semiconductor (MOS) transistor;

wherein the second polysilicon layer comprises an emitter of the double poly bipolar transistor and a source/drain and a deep collector of the double poly MOS transistor;

wherein the extrinsic base of the double poly bipolar transistor comprises a first dopant having a first dopant concentration, and wherein the gate of the double poly MOS transistor comprises the first dopant having the first dopant concentration;

wherein the emitter of the double poly bipolar transistor comprises a second dopant having a second dopant concentration, and wherein the source/drain of the double poly MOS transistor comprises the second dopant having the second dopant concentration; and

wherein the semiconductor substrate comprises a first region having a third dopant forming an intrinsic base of the double poly bipolar transistor and a second region having the third dopant forming a lightly doped drain of the double poly MOS transistor.